Amendments to the Claims:

Please amended claims 1 and 14 and cancel claims 11 and 13 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device comprising a silicon-containing semiconductor body with a surface, which semiconductor body is provided, near the surface thereof, with a transistor comprising: a gate situated at the surface and having a side wall spacer on either side of the gate, and further comprising, on either side of the gate, a diffusion region formed in the semiconductor body, at least one diffusion region being provided at the surface of the semiconductor body with a silicide region, characterized in that the silicide region extends along the surface of the semiconductor body and continues for more than 10 nm under the side wall spacer, wherein the side wall spacer is L-shaped and comprises a first portion, which borders on the gate and extends substantially perpendicularly with respect to the surface of the semiconductor body, and a second portion which extends along the surface of the semiconductor body, wherein the silicide region is completely below the side wall spacer, wherein the side wall spacer is configured to directly contact the entire surface of a side of the gate, and wherein the side wall spacer is made of one material.

2. (previously presented) A semiconductor device as claimed in claim 1, characterized in that the silicide region contains a metal which, in the silicide region formed, has a higher diffusion rate than silicon.

3. (previously presented) A semiconductor device as claimed in claim 2, characterized in that the metal is selected from the group comprising nickel (Ni), platinum (Pt) and palladium (Pd) and alloys of these metals.

4. (canceled)

5. (previously presented) A semiconductor device as claimed in claim 1, characterized in that the second portion of the L-shaped side wall spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of maximally 40 nm.

6. (previously presented) A semiconductor device as claimed in claim 1, characterized in that an insulating layer extends in the semiconductor body in a direction parallel to the surface of the semiconductor body.

7. (previously presented) A semiconductor device as claimed in claim 1, characterized in that the semiconductor body comprises a germanium component.

8. (previously presented) A semiconductor device as claimed in claim 1, characterized in that the semiconductor body comprises a strained-silicon layer.

9. (previously presented) A semiconductor device as claimed in claim 1, characterized in that the at least one diffusion region comprises the silicide region.

10. (previously presented) A semiconductor device as claimed in claim 1, characterized in that the at least one diffusion region comprises a diffusion region extension, the silicide region comprising a silicide region extension, the silicide region extension falling completely within the diffusion region extension.

11. (canceled)

12. (previously presented) A semiconductor device as claimed in claim 2, characterized in that the metal is palladium (Pd).

13. (canceled)

14. (currently amended) A semiconductor device as claimed in claim 1, wherein the side wall spacer is configured to contact the entire surface of ~~a~~ the side of the gate without an intervening structure.

15. (previously presented) A semiconductor device as claimed in claim 1 further comprising an insulation layer that is located below the gate, wherein the side wall spacer is configured to directly contact the insulation layer.

16. (previously presented) A semiconductor device as claimed in claim 1 further comprising an insulation layer that is located below the gate, wherein the gate comprises a conductive layer and a silicide layer, and wherein the side wall spacer is configured to directly contact the insulation layer, the conductive layer and the silicide layer.

17. (previously presented) A semiconductor device as claimed in claim 1 further comprising an insulation layer that is located below the gate, wherein the gate comprises a metal conductive layer, and wherein the side wall spacer is configured to directly contact the insulation layer and the metal conductive layer.

18. (previously presented) A semiconductor device as claimed in claim 1 further comprising an insulation layer that is located below the gate, wherein the gate comprises a conductive layer that is made of polycrystalline silicon, and wherein the side wall spacer is configured to directly contact the insulation layer and the conductive layer.

19. (previously presented) A semiconductor device as claimed in claim 1, wherein the second portion of the L-shaped side wall spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of 5 to 20 nm.

20. (previously presented) A semiconductor device as claimed in claim 1, wherein the silicide region contains a metal which, in the silicide region formed, has a higher diffusion rate than silicon, and wherein the second portion of the L-shaped side wall

spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of maximally 40 nm.

21. (previously presented) A semiconductor device as claimed in claim 1, wherein the silicide region contains a metal which, in the silicide region formed, has a higher diffusion rate than silicon, and wherein an insulating layer extends in the semiconductor body in a direction parallel to the surface of the semiconductor body.